



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,091	08/28/2001	Tae-sung Jung	5649-886	5816
20792	7590	08/07/2006	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC			CAO, CHUN	
PO BOX 37428			ART UNIT	
RALEIGH, NC 27627			PAPER NUMBER	
			2115	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/941,091

Applicant(s)

JUNG ET AL.

Examiner

Chun Cao

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30,34,35,37,43 and 44 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 34,35 and 37 is/are allowed.
- 6) ☒ Claim(s) 1-25,27-30,43 and 44 is/are rejected.
- 7) ☒ Claim(s) 26 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

FINAL REJECTION

1. Claims 1-30, 34, 35, 37, 43 and 44 are presented for examination.
2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.
3. The rejections are respectfully maintained and reproduced infra for applicant's convenience.
4. Claims 3-11 are rejected under 35 U.S.C. 102(e) as being anticipated by McClannahan (McClannahan), U.S. patent no. 6,438,670.

As per claim 3, McClannahan discloses that a memory controller for controlling memory modules [74, 74a, fig. 5], into which a plurality of semiconductor memory devices [76, fig. 5] are loaded, comprising:

a module selector [84, fig. 6] for outputting a module selection signal for selecting the memory modules in response to a clock signal [col. 9, lines 18-23];

a delay control register for receiving delay control information according to a specification from serial presence detectors (SPD) loaded into the memory modules and storing the received delay control information [fig. 1; col.6, lines 8-13; col. 8, lines 38-51; emphasis added, "the memory storage devices may have one or more timing parameter providing minimum delays..."]; and

an output buffer for delaying an internal command signal, an internal address signal, and write data in response to the output signal of the module selector and outputting the delayed write data to the semiconductor memory device [fig. 6; col. 8, lines 53-66];

wherein the delay time of the output buffer is controlled in response to the output signal of the delay control register [col. 5, lines 50-52, 61-63; col. 6, lines 19-29; figures 10, 11].

McClannahan does not explicitly disclose a delay control register for receiving delay control information according to a specification from serial presence detectors (SPD) loaded into the memory modules.

As per claim 4, McClannahan discloses the memory controller further comprises an input buffer, whose delay time is controlled in response to the output signal of the delay control register, the input buffer for delaying read data received from the semiconductor memory device and outputting the delayed read data to the inside of the memory controller [fig. 6; col. 8, lines 53-66].

As per claim 5, McClannahan inherently teaches that a first signal for selecting a memory module, which does not need a predetermined delay time; and a second signal for selecting a memory module, which need the predetermined delay time [fig. 6; col. 8, line 53-col. 9, line 36].

As per claim 6, McClannahan discloses that the output buffer comprises:

a delay controller for receiving the output signal of the delay control register and the second signal and setting the predetermined delay time; a command output buffer for delaying a command signal in response to the output signal of the delay controller and the first signal; an address output buffer for delaying an address signal in response to the output signal of the delay controller and the first signal; and a data output buffer

for delaying write data in response to the output signal of the delay controller and the first signal [fig. 6, col. 8, line 53-col. 9, line 36].

As per claim 7, McClannahan discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to an output signal of the delay control register [col.6, lines 8-13; col. 8, lines 49-51]; and a data input buffer for delaying read data received from the semiconductor memory device and outputting the delayed read data to the inside thereof in response to the output signal of the delay controller [figures 6, 7; col. 8, lines 53-66].

As to claims 8-11 are written mean plus function and contained the same limitations as set forth in claims 3-7. Therefore, same rejection is applied.

5. Claims 1, 2, 12-25, 27-30 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClannahan (McClannahan), U.S. patent no. 6,438,670 in view of Keeth et al. (Keeth), U.S. patent no. 6,101,197.

As per claim 1, McClannahan discloses that a semiconductor memory device controlled by a memory controller [fig. 5], comprising:

the memory controller having a delay control register [26, fig. 1] for receiving delay control information and storing the received delay control information [fig. 1; col.6, lines-13; col. 8, lines 49-51]; and

McClannahan does not explicitly disclose the semiconductor memory device having a delay control register for receiving delay control information from the memory controller.

Keeth discloses a delay control register [204, fig. 4] for receiving delay control information from the memory controller [col. 1, lines 51-54; col. 18, lines 6-9; fig. 7] and storing the information; and an input buffer for receiving a command signal, an address signal, and write data from the memory controller and delaying the received command signal, address signal, and write data; wherein a delay time of the input buffer is controlled in response to an output signal of the delay control register [figures 3, 4; col. 7, lines 11-41; col. 8, lines 1-49].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of McClannahan and Keeth because they are both directed to a memory device system, and the specify teachings of Keeth stated above would improve the efficiency of operation and reduce signal skew of the memory device of McClannahan by having a delay control register stored delay control information in the memory device.

As per claim 2, Keeth discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to the output signal of the delay control register; a data input buffer for delaying the write data in response to the output signal of the delay controller; an address input buffer of delaying the address signal in response to the output signal of the delay controller; and a command input buffer for delaying the command signal in response to the output signal of the delay controller [figures. 2-4; col. 6, line 27-col. 7, line 6; col. 7, line 11-col. 8, line 49].

As per claim 12, Keeth discloses a delay control register [204, fig. 4] for receiving delay control information from the memory controller [col. 1, lines 51-54] and storing the

information; and an input buffer for receiving a command signal, an address signal, and write data from the memory controller and delaying the received command signal, address signal, and write data; wherein a delay time of the input buffer is controlled in response to an output signal of the delay control register [figures 3, 4; col. 7, lines 11-41; col. 8, lines 1-49].

As per claim 13, Keeth discloses that the input buffer comprises: a delay controller for setting a predetermined delay time in response to the output signal of the delay control register; a data input buffer for delaying the write data in response to the output signal of the delay controller; an address input buffer of delaying the address signal in response to the output signal of the delay controller; and a command input buffer for delaying the command signal in response to the output signal of the delay controller [figures. 2-4; col. 6, line 27-col. 7, line 6; col. 7, line 11-col. 8, line 49].

As to claims 14-23 and 43-44, McClannahan and Keeth basically teach the corresponding elements as set forth in claims 1-13 that are carried out the method of operating steps in claims 14-23 and 43-44. McClannahan and Keeth teach the claimed system. Therefore, McClannahan and Keeth teach the claimed method of steps to carry out the system.

As to claims 24, 25 and 27-30 are written mean plus function and contained the same limitations as set forth in claims 1-13. Therefore, same rejection is applied.

Allowable Subject Matter

6. Claim 26 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 34, 35 and 37 are allowed over prior art.

8. Applicant's arguments filed on 6/19/06, which have been fully considered but they are not persuasive. Applicant's arguments with respect to claims 1-30, 34, 35, 37, 43 and 44 have been considered but are moot in view of rejection indicated above.

9. In the remarks, applicants argued in substance that 1) Keeth does not teach or suggest in Keeth that the memory array 180 shown in FIG. 3 of Keeth can receive and/or store delay control information. 2) McClannahan does not teach that receives delay control information from one or more memory modules, and delay control information is stored in SPDs that are loaded into the memory modules.

10. The examiner respectfully traverses. As to 1) While the examiner agreed with applicant's position. However, Keeth discloses the limitation as set forth in the claim, such as "a delay control register [204, fig. 4] for receiving delay control information from the memory controller and storing the information [col. 1, lines 51-54; col. 18, lines 6-9; fig. 7]"; and the storage register 204 of Keeth is part of the memory device 162 [see figures 3 and 4]. As to 2), McClannahan teaches that receives delay control information from one or more memory modules, and delay control information is stored in SPDs that are loaded into the memory modules [fig. 1; col.6, lines 8-13; col. 8, lines 38-51;

emphasis added, "the memory storage devices may have one or more timing parameter providing minimum delays..."].

See rejection indicated above.

11. **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Art Unit: 2115

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Aug. 3, 2006

CHUN CAO
PRIMARY EXAMINER